Device Features

- Low power 1.8V operation
- Small footprint in 96-Ball VFBGA Package (6x6mm)
- Fully qualified Bluetooth component
- 0.18µm CMOS technology
- Full speed class 2 Bluetooth operation with full 7 slave piconet support
- Support for 8Mbit external Flash
- Minimum external components
- Operates over full industrial temperature range (-40≤T≤105°C)

BlueCore™2-External

Single Chip Bluetooth System

Pre-Production Information Data Sheet
BC212013A
(UART only version)
BC212015A
(USB and UART version)

October 2001

General Description

BlueCore2-External is a single chip radio and baseband IC for Bluetooth 2.4GHz radios implemented in CMOS technology.

When used with external ROM containing the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system for data and voice communications.

Applications

- PC Notebooks
- Cellular Handsets
- Cordless Headsets
- Personal Digital Assistants (PDAs)
- Computer Accessories (Compact Flash, PCMCIA and SD cards)

The design is optimised to require few external RF components to facilitate rapid design of the application printed circuit board and therefore the fastest possible time to market and lowest overall cost.

Included in the device are autocalibration and built-in-self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification.

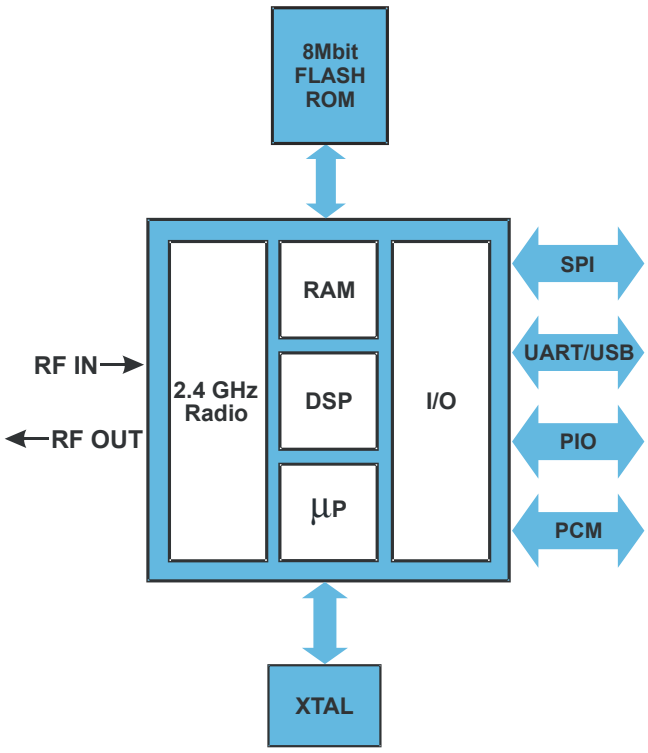


Figure 1: BlueCore2-External System Architecture

Key Features

Radio

- No external trimming is required in production
- Operation with common TX/RX terminals simplifies external matching circuitry and eliminates external antenna switch
- Extensive built-in-self-test minimises end product final test time
- Full RF reference designs are available

Transmitter

- Up to +4dBm RF transmit power with level control from the on-chip 6-bit DAC over a dynamic range greater than 30dB
- Supports Class 2 and Class 3 radios without the need for an external power amplifier or TX/RX switch
- Supports Class 1 radios with an external power amplifier provided by a power control terminal controlled by an internal 8-bit voltage DAC and by control of an external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for better sensitivity and co-channel rejection
- Digitised RSSI available in real time over the HCI
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser: no external VCO varactor diode or resonator
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz), or an external clock

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands and an integrated low power oscillator for ultra-low Park/Sniff/Hold mode power consumption
- Device can be used with an external master oscillator and provides a ‘clock request signal’ to control external clock source

Baseband and Software

- External 8Mbit Flash ROM for complete system solution and application flexibility
- 32Kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full 7 slave piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bitstream generation, whitening and transmit pulse shaping
- Trancoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for software debugging
- UART interface with programmable baud rate up to 1.5Mbaud
- Full speed USB interface supports OHCI and UHCI compliant with USB v1.1
- Synchronous bidirectional serial programmable audio interface
- Optional I^2C compatible interface

Bluetooth Stack Running on Internal Microcontroller

CSR’s Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM, thus reducing host CPU load
- Stand-alone single chip (no host) including virtual machine (VM) programming environment, for instance for headsets and PC peripherals

More information on the CSR Bluetooth Software Stack and software development tools is available in separate documentation from CSR.

Package Options

- 96-Ball VFBGA 8x8x1.0mm 0.65mm Pitch
- 96-Ball VFBGA 6x6x1.0mm 0.5mm Pitch

Device Diagram

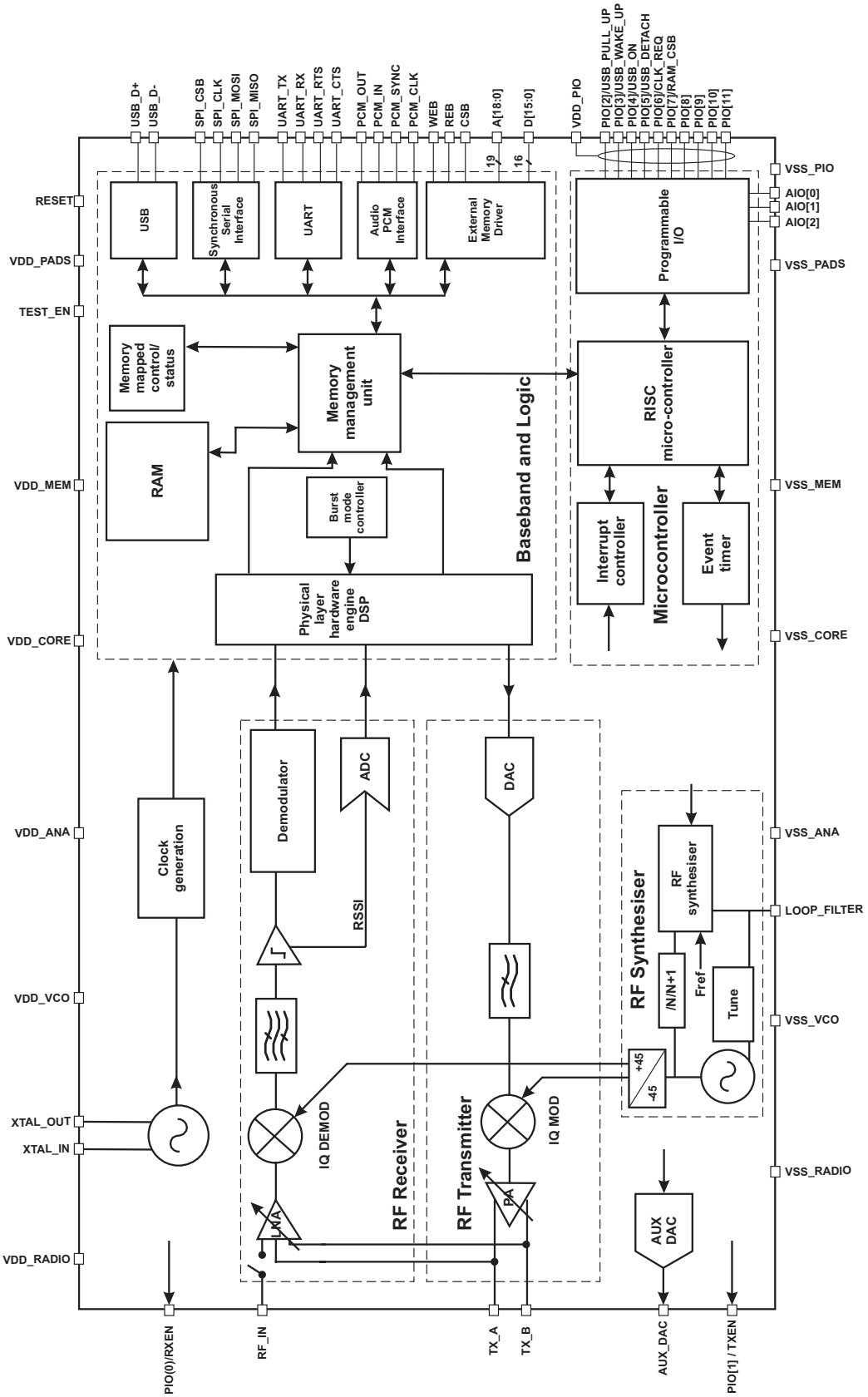
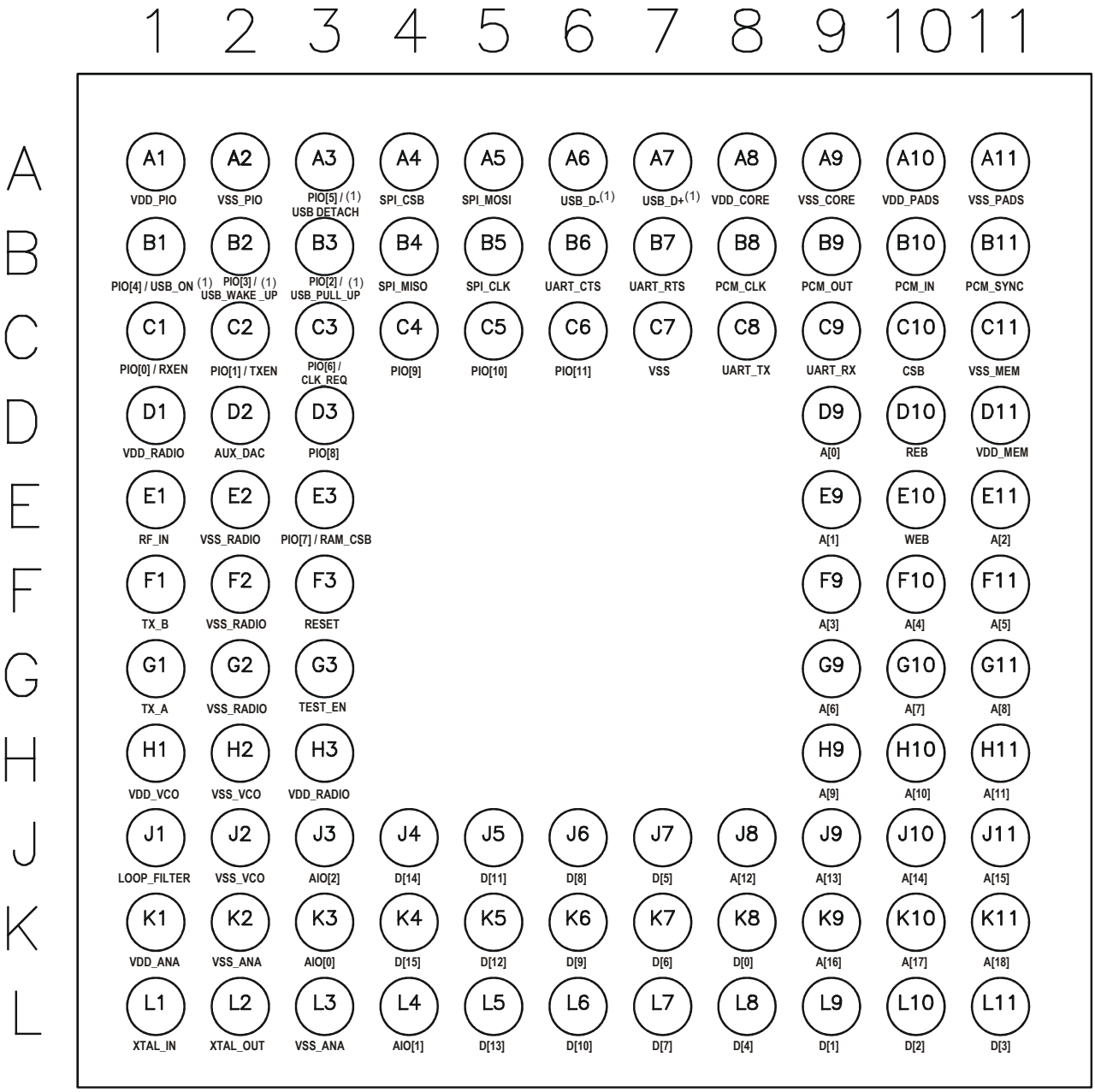


Figure 2: BlueCore2-External Device Diagram

Device Pinout Diagram(2)

Orientation from top of device



Note:
(1) USB functions are available on BC212015A only.
(2) Device pinout diagram is the same for both 8x8x1mm package (DN) and 6x6x1mm package (EN).

Figure 3: BlueCore2-External Device Pinout

Device Terminal Functions

Terminal Name	Pad Type	Ball	Description
Radio			
RF_IN	Analog	E1	Single ended receiver input
PIO[1] / TXEN	Bidirectional with weak internal pull-up/down	C2	Control output for external PA Class 1 only (=PIO[1])
PIO[0] / RXEN	Bidirectional with weak internal pull-up/down	C1	Control output for external LNA (if fitted) (=PIO[0])
TX_A	Analog	G1	Transmitter output/Switched Receiver input
TX_B	Analog	F1	Complement of TX_A
AUX_DAC	Analog	D2	Voltage DAC output
Synthesiser and Oscillator			
XTAL_IN	Analog	L1	For crystal or external clock input
XTAL_OUT	Analog	L2	Drive for crystal
LOOP_FILTER	Analog	J1	Connection to external PLL loop filter
External Memory Port			
REB	CMOS output, tristatable with internal weak pull-up	D10	Read enable for external memory (active low)
WEB	CMOS output, tristatable with internal weak pull-up	E10	Write enable for external memory (active low)
CSB	CMOS output, tristatable with weak internal pull-up	C10	Chip select for external memory (active low)
A[18:0]	CMOS output	(1)	Address lines
D[15:0]	Bidirectional with weak internal pull-down	(1)	Data bus
PCM Interface			
PCM_OUT	CMOS output, tristatable with weak internal pull-down	B9	Synchronous data output
PCM_IN	CMOS input with weak internal pull-down	B10	Synchronous data input
PCM_SYNC	Bidirectional with weak internal pull-down	B11	Synchronous data strobe
PCM_CLK	Bidirectional with weak internal pull-down	B8	Synchronous data clock
USB and UART			
UART_TX	CMOS output	C8	UART data output
UART_RX	CMOS input with weak internal pull-down	C9	UART data input
UART_RTS	CMOS output, tristatable with internal weak pull-up	B7	UART ready to send
UART_CTS	CMOS input with weak internal pull-down	B6	UART clear to send
USB_D+ (2)	Bidirectional	A7	USB data plus
USB_D- (2)	Bidirectional	A6	USB data minus

Note:
(1) See Address and Data Bus tables at the end of this section.
(2) These terminals are available on BC212015A only.

Terminal Name	Pad Type	Ball	Description
Test and Debug			
RESET	CMOS input with weak internal pull-down	F3	Reset if high
SPI_CSB	CMOS input with weak internal pull-up	A4	Chip select for Synchronous Serial Interface
SPI_CLK	CMOS input with weak internal pull-down	B5	Synchronous Serial Interface Clock
SPI_MOSI	CMOS input with weak internal pull-down	A5	Synchronous Serial Interface data input
SPI_MISO	CMOS output, tristatable with weak internal pull-down	B4	Synchronous Serial Interface data output
TEST_EN	CMOS input with strong internal pull-down	G3	For test purposes only (leave unconnected)
PIO Port			
PIO[2] /USB_PULL_UP (1)	Bidirectional with programmable weak internal pull-up/down	B3	PIO or USB pull-up (via 1.5kΩ resistor to USB_D+)
PIO[3] /USB_WAKE_UP (1)	Bidirectional with programmable weak internal pull-up/down	B2	PIO or Output goes high to wake up PC when in USB mode
PIO[4] /USB_ON (1)	Bidirectional with programmable weak internal pull-up/down	B1	PIO or USB on (input senses when VBUS is high, wakes BlueCore2-External)
PIO[5] / USB_DETACH (1)	Bidirectional with programmable weak internal pull-up/down	A3	PIO line or chip detaches from USB when this input is high
PIO[6] / CLK_REQ	Bidirectional with programmable weak internal pull-up/down	C3	PIO line or clock request for external clock line
PIO[7] / RAM_CSB	Bidirectional with programmable weak internal pull-up/down	E3	Programmable Input/Output line
PIO[8]	Bidirectional with programmable weak internal pull-up/down	D3	Programmable Input/Output line
PIO[9]	Bidirectional with programmable weak internal pull-up/down	C4	Programmable Input/Output line
PIO[10]	Bidirectional with programmable weak internal pull-up/down	C5	Programmable Input/Output line
PIO[11]	Bidirectional with programmable weak internal pull-up/down	C6	Programmable Input/Output line
AIO[0]	Bidirectional	K3	Programmable Input/Output line
AIO[1]	Bidirectional	L4	Programmable Input/Output line
AIO[2]	Bidirectional	J3	Programmable Input/Output line

Note:
(1) USB functions are available on BC212015A only.

Power Supplies and Control			
VDD_RADIO	VDD	D1, H3	Positive supply connection for RF circuitry
VDD_VCO	VDD	H1	Positive supply for VCO and synthesiser circuitry
VDD_ANA	VDD	K1	Positive supply for analogue circuitry
VDD_CORE	VDD	A8	Positive supply for internal digital circuitry
VDD_PIO	VDD	A1	Positive supply for PIO & AUX DAC
VDD_PADS	VDD	A10	Positive supply for all other Input/Output
VDD_MEM	VDD	D11	Positive supply for external memory port & AIO
VSS_RADIO	VSS	E2, F2,G2	Ground connections for RF circuitry
VSS_VCO	VSS	J2, H2	Ground connections for VCO and synthesiser
VSS_ANA	VSS	L3, K2	Ground connections for analogue circuitry
VSS_CORE	VSS	A9	Ground connection for internal digital circuitry
VSS_PIO	VSS	A2	Ground connection for PIO & AUX DAC
VSS_PADS	VSS	A11	Ground connection for Input/Output except memory port
VSS_MEM	VSS	C11	Ground connection for external memory port
VSS	VSS	C7	Ground connection for internal package shield

Address Lines	
Terminal	Ball
A[0]	D9
A[1]	E9
A[2]	E11
A[3]	F9
A[4]	F10
A[5]	F11
A[6]	G9
A[7]	G10
A[8]	G11
A[9]	H9
A[10]	H10
A[11]	H11
A[12]	J8
A[13]	J9
A[14]	J10
A[15]	J11
A[16]	K9
A[17]	K10
A[18]	K11

Data Bus	
Terminal	Ball
D[0]	K8
D[1]	L9
D[2]	L10
D[3]	L11
D[4]	L8
D[5]	J7
D[6]	K7
D[7]	L7
D[8]	J6
D[9]	K6
D[10]	L6
D[11]	J5
D[12]	K5
D[13]	L5
D[14]	J4
D[15]	K4

Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	-0.4V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	-0.4V	3.6V
Other Terminal Voltages (except 5V tolerant)	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature range	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	1.70V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	1.70V	3.60V

Input/Output Terminal Characteristics

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise
VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low (VDD=3.0V)	-0.4	-	+0.8	V
(VDD=1.8V)	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Input Current				
TEST_EN input high I_{IH}	+10	-	+200	µA
SPI_CSB input low I_{IL}	-5	-	-1	µA
PIO with pull up selected input low I_{IL}	-5	-	-1	µA
All other inputs, in any state I_I ($0V \le V_{IN} < V_{DD}$)	-1	-	+5	µA
Output Voltage				
V_{OL} output logic level low, (I_O = 4.0mA), VDD=3.0V	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA), VDD=1.8V	-	-	0.4	V
V_{OH} output logic level high, (I_O = 4.0mA), VDD=3.0V	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = 4.0mA), VDD=1.8V	VDD-0.4	-	-	V
Tri-state Leakage Current (See input current except for) SPI_MISO, PCM_OUT, UART_RTS CSB, WEB, REB: (VDD=3.0V)	-1	-	+5	µA
(VDD=1.8V)	-1	-	+2	µA
C_I Input Capacitance	2.5	-	10	pF

Note:
Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

Input/Output Terminal Characteristics (continued)				
Power-on Reset	**Min**	**Typ**	**Max**	**Unit**
VDD falling threshold VDD rising threshold Hysteresis	- - -	1.4 1.6 0.2	- - -	V V V
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
Input threshold V_{IL} input logic level low V_{IH} input logic level high	 - 0.7VDD_PADS	 - -	 0.3VDD_PADS -	 V V
Input leakage current, VSS_PADS<V_{IN}<VDD_PADS	-1	-	1	µA
C_I Input Capacitance	2.5	-	10	pF
Output levels to correctly terminated USB cable V_{OL} output logic level low V_{OH} output logic level high	 0 2.8	 - -	 0.2 VDD_PADS	 V V
Auxiliary DAC	**Min**	**Typ**	**Max**	**Unit**
Resolution Output Step Size		 13	8	bits mV
Output voltage Voltage range (I_O = 0) Current range Minimum output voltage (I_O = 200µA) Maximum output voltage (I_O = -10mA) Tristate leakage current	 VSS_PIO -10 0 VDD_PIO-0.3 -1	 - - - - -	 VDD_PIO +0.2 0.2 VDD_PIO +1	 V mA V V µA
Accuracy Gain Error Offset Linearity Settling Time (50pF load)		 ±5% ±3 Monotonic 5		 LSB µs
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency (1)	8.0	-	32.0	MHz
Digital trim range (1) (2)	5	6.2	8	pF
Trim step size (2)	-	0.1	-	pF
Negative tranconductance	2.0	-	-	mS

Note:
(1) Integer multiple of 250kHz.
(2) The difference between the local capacitance at minimum and maximum settings of the internal digital trim.The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

Radio Characteristics

VDD = 1.8V Temperature = 20˚C Frequency=2.441GHz

Receiver	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER (1)	-	-85	-	≤-70	dBm
Maximum received signal at 0.1% BER(1)	-	-5.0	-	≥-20	dBm
C/I Co-channel (1)	-	9	-	≤11	dB
Adjacent channel selectivity C/I 1MHz (1)	-	-2.0	-	≤0	dB
2nd adjacent channel selectivity C/I 2MHz (1)	-	-34	-	≤-30	dB
3rd adjacent channel selectivity C/I ≥3MHz (1) (2)	-	-43	-	≤-40	dB
Image rejection C/I (1) (3)	-	-12	-	≤-9	dB
Maximum level of intermodulation interferers (1) (4)	-	-30	-	≤-39	dBm
Maximum level of GSM signal at 1.8GHz (5)	-	-7	-	-	dBm
Maximum level of W-CDMA signal at 1.8GHz (5)	-	-9.5	-	-	dBm
Maximum level of W-CDMA signal at 2.2GHz (5)	-	-11	-	-	dBm

Transmitter	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power (1)	-	7.0	-	-6 to +4	dBm
RF power control range (1)	-	30	-	≥16	dB
RF power range control resolution	-	2.0	-	-	dB
20dB bandwidth for modulated carrier	-	900	-	≤1000	kHz
2nd adjacent channel transmit power (1)	-	-52	-	≤-20	dBm
3rd adjacent channel transmit power (1)	-	-57	-	≤-40	dBm

Notes:

(1) Measured according to the Bluetooth specification.

(2) Up to five spurious responses within Bluetooth limits are allowed.

(3) At carrier -3MHz.

(4) Measured at f_1-f_2=5MHz.

(5) For 0.1% BER with wanted input at -67dBm, and with the RF filter removed from the circuit.

Results shown are referenced to input of the RF balun.

Current Consumption(1)

VDD = 1.8V Temperature = 20˚C

Mode	Avg	Peak	Unit
SCO connection HV3 (1s interval sniff mode) (Slave)	28	-	mA
SCO connection HV3 (1s interval sniff mode) (Master)	28	-	mA
SCO connection HV1 (Slave)	53	-	mA
SCO connection HV1 (Master)	53	-	mA
ACL data transfer 115.2kbps UART (Master)	15	-	mA
ACL data transfer 720kbps USB (Slave)	61	-	mA
ACL data transfer 720kbps USB (Master)	61	-	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4	-	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	-	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	-	mA
Deep Sleep Mode	15	-	µA
Peak RF current during RF burst	80	-	mA

Note:

(1) Current consumption is for BC212015A and includes current supplied to external 3V Flash ROM. 1.8V Flash ROM will further reduce this figure.

Description of Functional Blocks

Radio Transceiver and Synthesiser

The receiver features a near-zero IF architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the LNA input allows the radio to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being de-sensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore2-External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection. Fast AGC is implemented by measuring the RSSI on a slot-by-slot basis and adjusting the front-end LNA gain to keep the first mixer input signal within a limited range. This improves the dynamic range of the receiver in interference-limited environments.

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot and results in a well controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

The maximum transmit power of +7dBm allows BlueCore2-External to be used in Class 2 and Class 3 radios and its support for transmit power control allows a simple implementation for Class 1 with an external RF power amplifier.

The radio synthesiser is fully integrated with no requirement for an external VCO screening can, varactor tuning diodes or LC resonators.

The radio has several built-in automatic calibration routines to maintain the radio performance within specification across temperature and ageing. No LNA , PA or TX/RX switch is required for Class 2 operation aross the device's full operating temperature range.

Auxiliary Features

The device contains two clock sources: one reference oscillator for the RF carrier frequency and one low frequency clock oscillator that is used as an interval timer during sleep modes, i.e., Sniff, Hold or Park.

The reference oscillator requires an external crystal. Alternatively, the crystal terminals can be driven from an external reference clock.The reference frequency can be in the range of 8-32MHz in multiples of 250kHz.

The low frequency clock oscillator requires no external components. It is calibrated automatically and maintains an accuracy of better than 250ppm. This oscillator consumes less than 2µA and is permanently enabled.

Physical Layer DSP Hardware Engine

Dedicated logic is used for forward error correction, header error control, cyclic redundancy check, encryption, data whitening, access code correlation and audio transcoding to translate between A-law, µ-law and linear voice data from the host and A-law, µ-law and Continuously Variable Slope Delta (CVSD) voice data over the air, voice interpolation for lost packets and rate mismatches are performed by the software.

Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in RAM. During radio receptions, the burst mode controller stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

Microcontroller, Interrupt Controller and Event Timer

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

Memory Management Unit

The memory management unit provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware memory management unit to minimise the overheads on the processor during data/voice transfers.

RAM

32Kbytes of on-chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

ROM

Up to 8Mbits of external Flash or masked programmed ROM (16 bit data words) can be attached giving maximum flexibility for running complete applications on chip. The ROM can be programmed over the synchronous serial/UART or USB interfaces after the device is mounted in the target application.

CSR Bluetooth Software Stack

BlueCore2-External is supplied with Bluetooth stack firmware that runs on its microcontroller and is resident in the external Flash memory. The stack occupies 4Mbits of storage.

The BlueCore Stack Software is compliant with the Bluetooth v1.1 specification. It implements all the features described in the specification, including optional features.

Piconets: up to seven slaves.

Power Saving: Hold, Sniff and Park

Data integrity: Channel Quality Driven Data Rate (CQDDR) and RSSI

Audio: full support for SCO

Role Switch: can reverse master/slave relationship

Device Firmware Upgrade

BlueCore2-External is supplied with boot loader software which implements a standard Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the external Flash memory through BlueCore2-External's UART/USB ports.

Additional Software for Host Implementation

A companion device, BlueCore2-PC can be ordered which includes software for a full Windows 98/ME or Windows 2000 Bluetooth host-side stack and application together with the IC hardware described in this datasheet. Contact CSR for more details.

Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore2-External a UART software driver is supplied that presents the HCI, L2CAP, RFCOMM and Service discovery APIs to higher Bluetooth stack layers running on the host. The code is provided as ‘C’ source or object code.

Other software drivers can be developed on request. Contact CSR Sales for more information.

Casira Development System

This is available to allow the evaluation of BlueCore2-External hardware and software and as the base of a toolkit for developing host software. Contact CSR Sales for more information.

Profiles Supported Via HCI

The supplied software stack is a full implementation of Bluetooth up to and including HCI, so all profiles and associated applications are supported.

Application Specific Software Development Environment

Firmware supplied with BlueCore2-External contains a protected user software execution environment as a Virtual Machine (VM). The user may write custom application code to run on the BlueCore VM using the BlueLab software development kit, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and BlueLab, the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code, including a full implementation of the headset profile.

External Interfaces

Transmitter/Receiver Inputs/Output

Terminals TX_A and TX_B form a balanced current output. They require a DC connection to VDD and should be connected through a balun to the antenna. The output impedance is capacitive and remains constant irrespective of whether the transmitter is enabled or disabled. For Class 2 operation these terminals also act as differential receive input terminals with an internal TX/RX switch.

For Class 1 operation the RF_IN ball is provided, which is single-ended and presents a capacitive input. A swing of up to 0.5V rms can be tolerated at this terminal. An external antenna switch can be connected to RF_IN.

Asynchronous Serial Data Port (UART) and USB Port

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous data serial port. The interface is designed to operate correctly when connected to other UART devices such as the NS16550A. The signalling levels are 0V and VDD_PADS. The interface is programmable over a variety of bit rates; no, even or odd parity; one or two stop bits and hardware flow control on or off. The default condition on power-up is pre-assigned in the external Flash memory.

The maximum UART data rate is 1.5Mbit/s. Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and is active low. UART_CTS is an input and is active low. These signals operate according to normal industry convention.

The port carries a number of logical channels: HCI data (both SCO and ACL), HCI commands and events, L2CAP API, RFCOMM API, Service Discovery API and device management. For the UART, these are combined into a robust tunnelling protocol, BlueCore Serial Protocol (BCSP), where each channel has its own software flow control and cannot block other data channels. In addition, the Bluetooth specification part H4 format is supported.

Alternatively a firmware version is available to support full speed (12Mbit/s) USB. USB_D+ and USB_D- are available on dedicated terminals. Both Open Host Controller Interface (OHCI) and Upper Host Controller Interfaces (UHCI) are supported.

The firmware in Flash can be downloaded through this port by DFU if the CSR-supplied boot loader is first programmed.

Firmware shipped with BlueCore2-External includes security features to prevent misuse of this upgrade facility.

PCM Codec Interface

PCM_OUT, PCM_IN, PCM_CLK, PCM_SYNC carry up to three bidirectional channels of voice data, each at 8 ks/s. The format of the PCM samples can be 8-bit A-law, 8-bit µ-law, 13-bit linear or 16-bit linear. The PCM_CLK and PCM_SYNC terminals can be configured as inputs or outputs depending on whether BlueCore2-External is the master or slave of the PCM interface.

BlueCore2-External interfaces directly to PCM audio devices such as the:
Qualcomm MSM 3000 series and **MSM 5000 series** CDMA devices,
OKI MSM7705 four channel µ/A-law codec,
Motorola MC145481 8-bit µ/A-law codec,
Motorola MC145483 13-bit linear codec and the
Mitel MT93LI6 Echo cancelling codec.

BlueCore2-External is also compatible with the Motorola SSI™ interface.

Synchronous Serial Port

BlueCore2-External is a slave device using terminals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CSB. This interface is used for program emulation/debug and IC test. It is also the means by which the external Flash ROM may be programmed ‘in situ’ before any 'boot' program is loaded. The designer should be aware that no security protection is built into the hardware or firmware associated with this port.

Parallel PIO Port

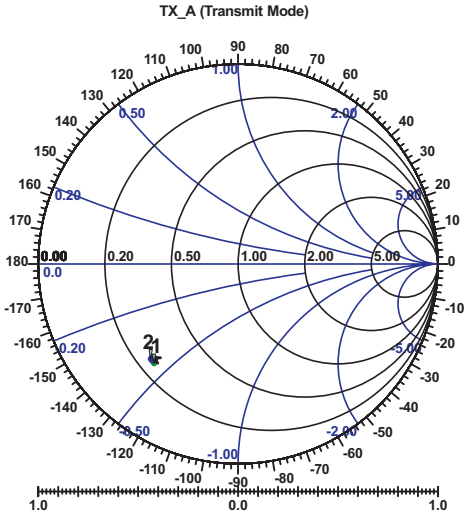
Fifteen lines of programmable bidirectional I/O are provided. PIO[11:0] are powered from VDD_PIO and AIO[2:0] are powered from VDD_MEM. PIO[0] and PIO[1] are normally dedicated to TXEN and RXEN, but they are available for general use. Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore2-External is provided from a system ASIC.

I^2C Interface

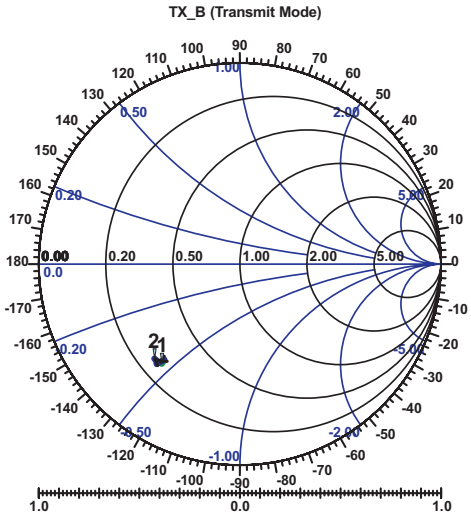
PIO[3] and PIO[2] can be used to form a master I^2C interface. The interface is formed using software to drive these lines and is thus suited only to relatively slow functions such as driving a dot matrix LCD display, a keyboard scanner or an EEPROM.

Application Information

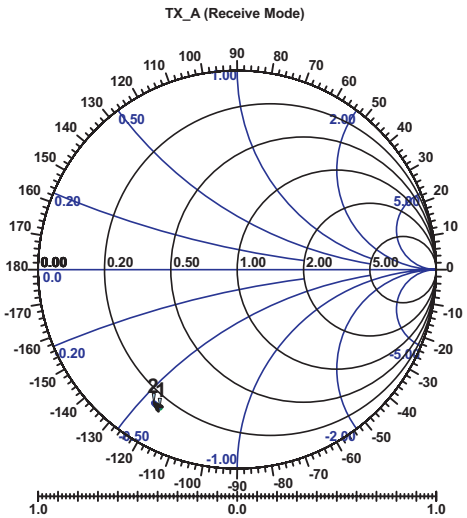
Transmit and receive port impedances for 8x8x1mm package



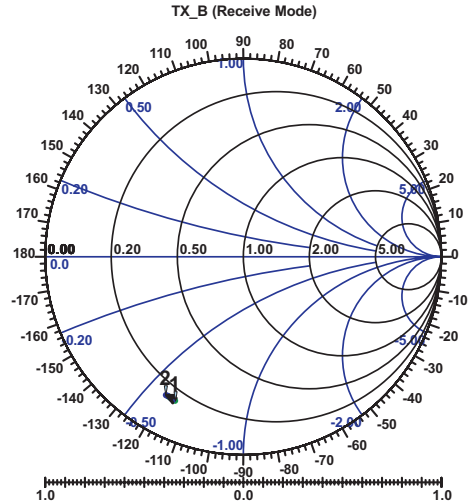
1: ZTTX_A(2402GHz) = (12.7 - j21.95)Ω
2: ZTTX_A(2480GHz) = (12.7 - j20.75)Ω



1: ZTTX_B(2402GHz) = (13.9 - j22.8)Ω
2: ZTTX_B(2480GHz) = (13.3 - j20.85)Ω



1: ZRTX_A(2402GHz) = (7.65 - j28.8)Ω
2: ZRTX_A(2480GHz) = (7.65 - j27.2)Ω



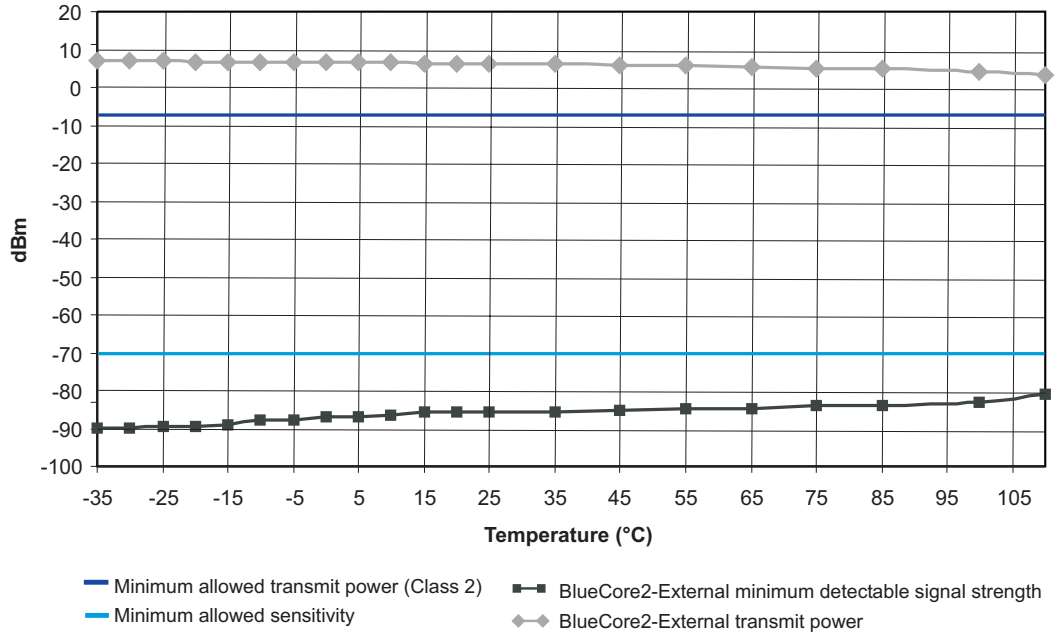
1: ZRTX_B(2402GHz) = (7.55 - j31.1)Ω
2: ZRTX_B(2480GHz) = (7.45 - j28.8)Ω

Note:
TX_A is in antiphase with TX_B.

ZTTX_A, ZTTX_B are the output impedances of ports TX_A and TX_B with BlueCore2-External in transmit mode.
ZRTX_A, ZRTX_B are the output impedances of ports TX_A and TX_B with BlueCore2-External in receive mode.

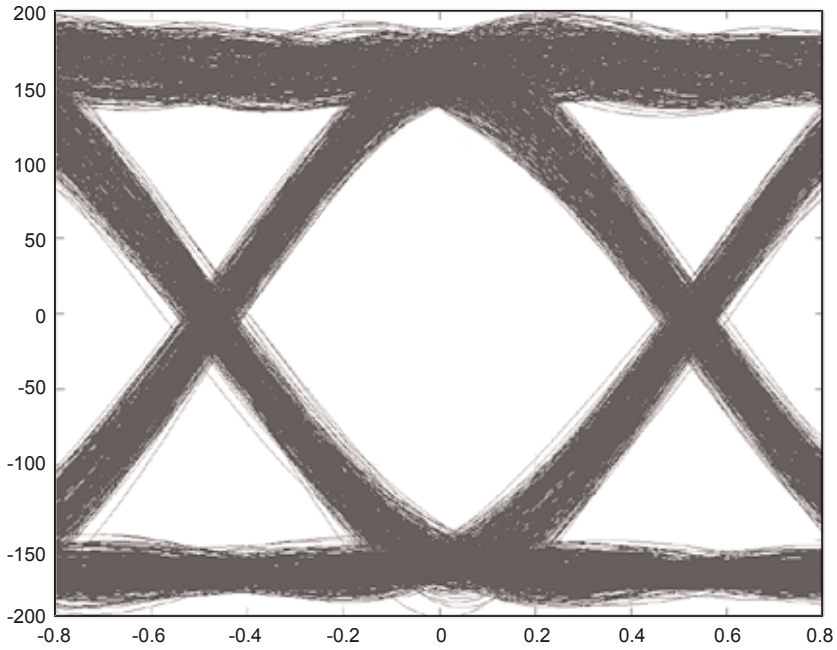
Figure 4: TX_A and TX_B Transmit and Receive modes impedance data

Typical Radio Performance



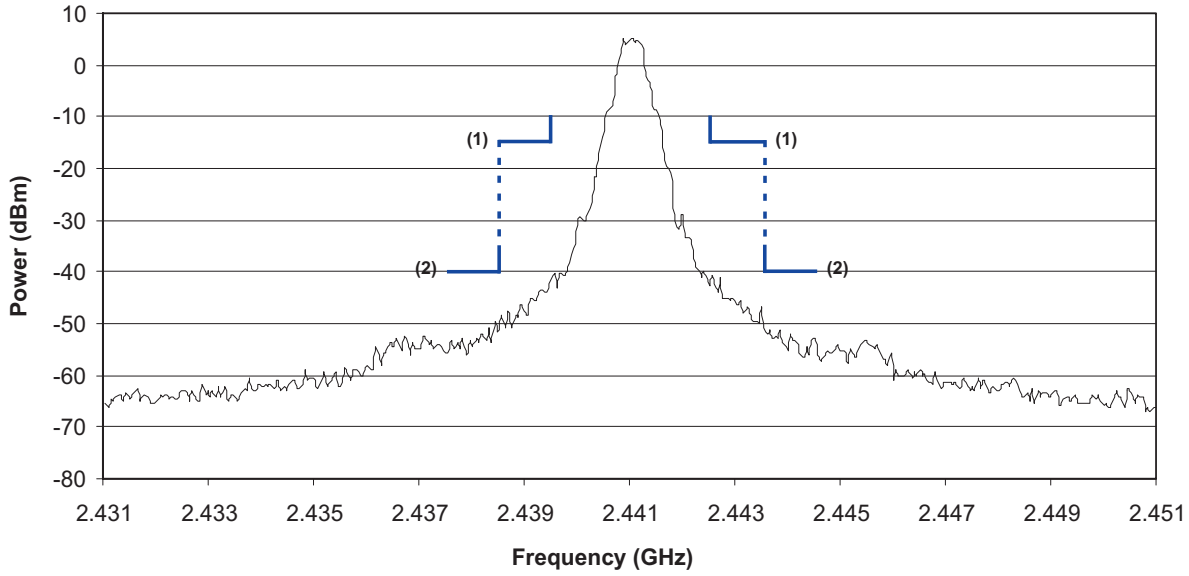
Note:
Results obtained using CSRs evaluation circuit, see figure 9.

Figure 5: Transmit power and receive sensitivity versus temperature



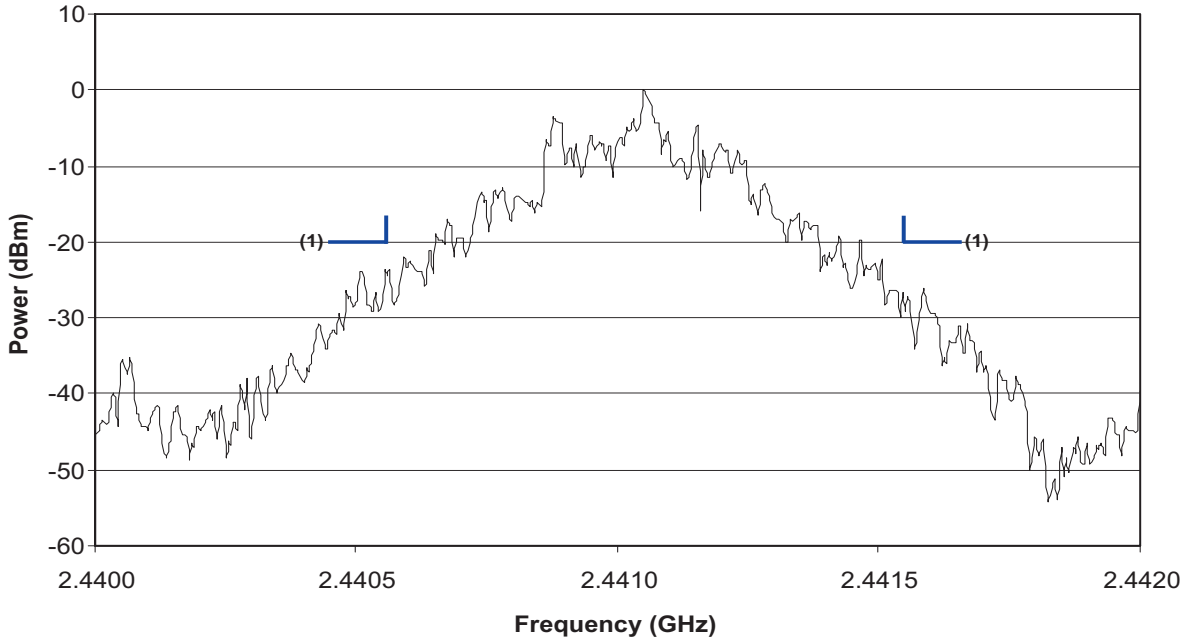
Notes:
Results obtained using CSRs evaluation circuit, see figure 9.
Transmit power: 7dBm.
Data: complete DH5 packet including pre-amble.
Temperature: 20°C.

Figure 6: Transmitter Eye Diagram



Notes:
(1) Maximum allowed adjacent channel power ($f=f_0 + 2MHz$).
(2) Maximum allowed adjacent channel power ($f=f_0 + 3MHz$).
Measurement resolution bandwidth = 100kHz.
Results obtained using CSR's evaluation circuit, see figure 9.
Temperature: 20°C.

Figure 7: Wideband transmit spectrum



Notes:
(1) Maximum allowed 20dB bandwidth.
Measurement resolution bandwidth = 10kHz.
Results obtained using CSR's evaluation circuit, see figure 9.
Temperature: 20°C.

Figure 8: Narrowband transmit spectrum

Evaluation Circuit

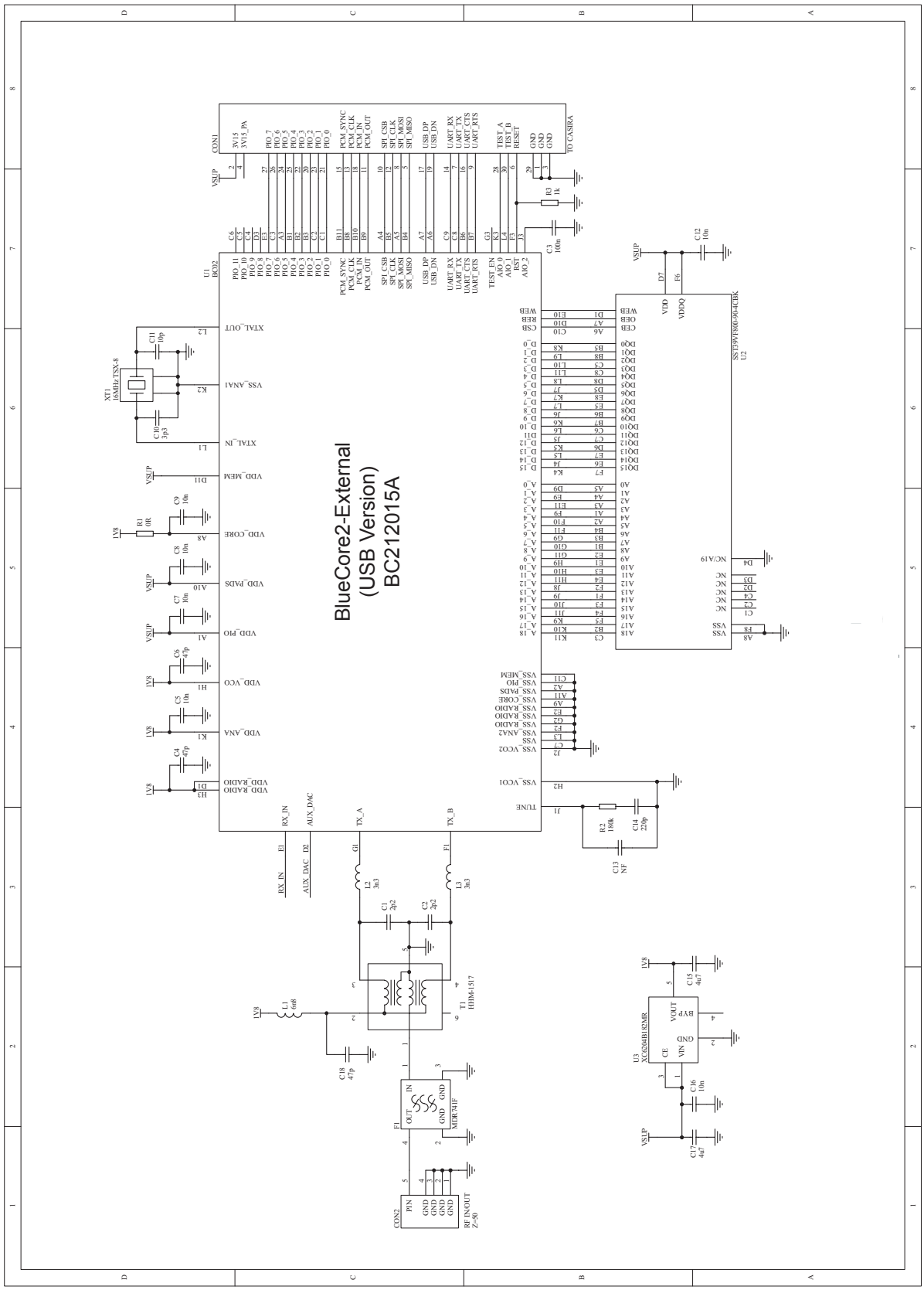
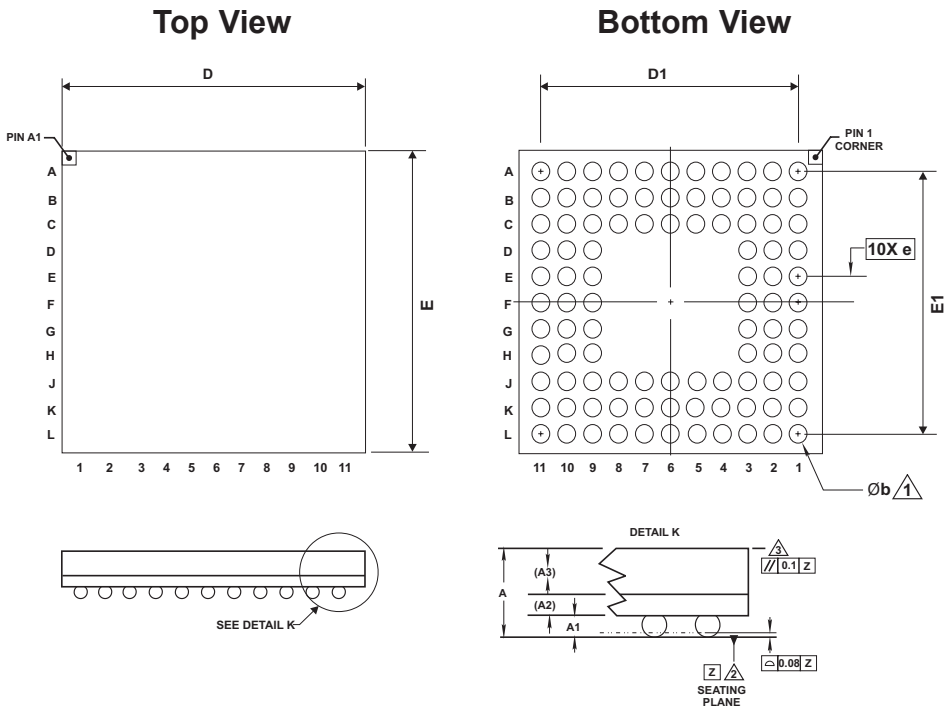


Figure 9: Evaluation circuit for BlueCore2-External module from which the data sheet test measurements were obtained

Package Dimensions



BC212015DN and BC212013DN 8x8x1mm VFBGA			
DIM	MIN	MAX	NOTES
A	0.8	1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2	0.3	
A2	0.22 REF		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.45 REF		
b	0.25	0.35	
D	8 BSC		3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
E	8 BSC		
e	0.65 BSC		
D1	6.5 BSC		
E1	6.5 BSC		
VFBGA 96 BALLS 8X8X1mm (JEDEC MO-225)			UNIT: MM

BC212015EN and BC212013EN 6x6x1mm VFBGA			
DIM	MIN	MAX	NOTES
A	0.8	1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2	0.3	
A2	0.22 REF		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.45 REF		
b	0.25	0.35	
D	6 BSC		3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
E	6 BSC		
e	0.5 BSC		
D1	5 BSC		
E1	5 BSC		
VFBGA 96 BALLS 6X6X1mm (JEDEC MO-225)			UNIT: MM

Figure 10: BlueCore2-External package dimensions

Ordering and Contact Information

Order Number	Package	Interface Version	Shipment Method
BC212015ADN-E4	8x8x1mm	USB and UART	Tape and reel
BC212015ADN-Y1	8x8x1mm	USB and UART	Tray (dry pack)
BC212013ADN-E4	8x8x1mm	UART only	Tape and reel
BC212013ADN-Y1	8x8x1mm	UART only	Tray (dry pack)
BC212015AEN-E4	6x6x1mm	USB and UART	Tape and reel
BC212015AEN-Y1	6x6x1mm	USB and UART	Tray (dry pack)
BC212013AEN-E4	6x6x1mm	UART only	Tape and reel
BC212013AEN-Y1	6x6x1mm	UART only	Tray (dry pack)

Packaging Options: 2Kpcs Taped & Reeled (E4)
348pcs Tray (5 Trays to a box) (Y1)

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To contact a CSR representative, please go to www.csr.com/contacts.htm

Status of Information

The progression of CSR Product Data Sheets follows the following format:

a) Advance Information
Information for designers on the target specification for a CSR product in development.
All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

b) Pre-Production Information
Final pinout and mechanical dimensions. All electrical specifications may be changed by CSR without notice.

c) Production Information
Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.
Production Data Sheets supersede all previous document versions.

The status of this Data Sheet is **Pre-Production Information.**

Life Support Policy and Use in Safety-Critical Applications
CSR's products are not authorised for use in life-support or safety-critical applications.

Date:	Revision:	Reason for Change:
September 2001	a	Latest information for BlueCore2-External
October 2001	b	Application information added

BlueCore2-External Product Data Sheet

BC212015-ds-001b

October 2001